IN THE CLAIMS

Claims 1 - 4 (Canceled)

5. (New) A method for performing a register renaming in a pipelined manner, for each group of instructions that are to go through a process of register renaming simultaneously, in a microprocessor based on superscalar architecture capable of out-of-order execution, comprising: physical registers; a free list that is designed to hold unallocated physical-register numbers; and a mapping table having entries that are provided in respective correspondence with a predetermined number of logical registers, the entries being each designed to hold a physical-register number, the method comprising the steps of:

(a) associating each logical-register number shown as a destination operand with a tag based on order of the instructions in the group, and associating each logical-register number shown as a source operand that is RAW (read-after-write) dependent on an instruction of the group with the same tag with which the destination operand of said instruction is being associated; and

(b) renaming each logical-register number associated with a tag to the physical-register number that is taken out of the free list and is allocated in correspondence with the associated tag, renaming each logical-register number associated with no tag to the physical-register number that is obtained by accessing the mapping table, and updating the mapping table in accordance with the group of instructions.

6. (New) The method for performing register renaming according to claim 5;

wherein both step (a) and step (b) take one cycle.

7. (New) The method for performing register renaming according to claim 5;

wherein step (a) takes multiple cycles, and step (b) takes one cycle.